IN THE CLAIMS

Please amend claim 31 as follows. All claims have been provided as a courtesy to the Examiner.

31. (Twice Amended) A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control the output of a status signal representing said protection status of a [said] data modification operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register [update at least one of said bits indicating said suspend status of said write operation in response to a suspend signal], and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine [control the output of said status signal in response to a status request signal].

32. (Unchanged) The memory device of claim 31, wherein said write operation represents a byte write operation.

33. (Unchanged) The memory device of claim 31, wherein said suspend signal represents a byte write suspend command.

34. (Unchanged) The memory device of claim 31, wherein said control circuit is to receive a status request signal and said register is to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (Unchanged) The memory device of claim 35, further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is to receive said status request signal from a processor and to provide said status signal to said processor.

36. (Unchanged) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is to provide a second status signal if said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (Unchanged) The memory device of claim 31, wherein said status request signal is a read status register command.